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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

7590 11/20/2002
ON Semiconductor
Patent Administration Dept - MD A700
P.O. Box 62890
Phoenix, AZ 85082-2890

EXAMINER

MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/072,145

Applicant(s)

AVERETT ET AL.

Examiner

Thomas J. Magee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) 12-25 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 1 – 11 in Letter No. 5 of September 12, 2002 is acknowledged.

Objections

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. In Figures 4 and 6, the "extra" layer (right side trench) lining the trench adjacent to the layer, 95, is not recited in the specification or in the claims. The origin or nature of this extra layer is unknown to Examiner. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application.

Claim Rejections – 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. '041 (US 5,640,041) in view of Lur et al. '786 (US 5,308,786).

Lur et al. '041 disclose a semiconductor device formed in a monocrystalline silicon sub-

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strate (Col. 3, line 67) where a second recessed region (22) (See Figure 6) is formed within a first recessed region (15,16) etched from a deposited silicon dioxide layer (Col. 4, lines 53 - 55) and the surface of trenches covered with silicon dioxide (CVD) (cap layer) to seal the "voids" or trenches (Col. 3, lines 10 - 15). The walls of trenches are covered with silicon dioxide (25) (See Figure 10).

Lur et al. '041 do not disclose that the second dielectric material (SiO_2) is thermally grown. However, for this application, a thermally grown and CVD silicon dioxide layer are functionally equivalent in terms of a sealant atop trenches.

An active device is formed in an active region (See Figure 14) with a gate dielectric (4), gate electrode (5), and doped regions (52,54) (n^+ , n^-) at the peripheral edges. An electrical (passive) component comprised of a bonding pad or electrode (5) over a dielectric region (3) containing "voids" is formed with electrical contacts (56) at the top.

Lur et al. '041 do not explicitly disclose the depth of trenches in the second recessed region. However, Lur et al. '786 disclose (Col. 4, lines 54 - 57) in a similar device for the narrow trenches (17) (See Figure 6) that the depth is 20,000 Angstroms (2 μm), which is consistent with the depth recited in the instant application, subject to optimization for a particular device application. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lur et al. '786 with Lur et al. '041 to obtain recesses of adequate depth for optimization of device parameters.

Conclusions

Any inquiry concerning this communication or earlier communications from the

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Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722**.

Thomas Magee
November 12, 2002

A handwritten signature in black ink that reads "Tom Thomas". The signature is written in a cursive style with a horizontal line above the name.

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800